A Novel Circuit-Level SEU Hardening Technique for High-Speed SiGe HBT Logic Circuits

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***Abstract*—In this work we present a new circuit-level hardening technique for SEU mitigation in high-speed SiGe BiCMOS digital logic. A reduction in SEU vulnerability is realized through the implementation of an additional storage cell redundancy block to achieve the required decoupling. When compared with latch duplication, current sharing or gated feedback techniques, this method incurs a lower power penalty and no speed penalty. The hardened circuit is implemented in CML and LVL families and circuit simulation models predict significant reduction in the number of upsets compared to the corresponding unhardened versions. The technique is also easy to incorporate into existing designs.**

***Index Terms*—Current mode logic (CML), low voltage logic (LVL), partial decoupling, silicon-germanium (SiGe), single event upset (SEU).**

I. Introduction

SILICON-GERMANIUM (SiGe) Heterojunction Bipolar Transistor (HBT) technology has generated considerable interest in the space community due to its III-V-like high-speed, Si-like integration capability, and inherent tolerance to multi-Mrad (SiO_2) levels of ionizing radiation, without any additional process hardening. This built-in total dose hardness, unfortunately, does not translate into improved single event upset (SEU) response for high-speed SiGe HBT digital logic [1], and substantial recent research (e.g., [2], [3]) has been aimed at improving SEU immunity in SiGe, culminating in the first successful hardening of SiGe logic using a combination of device and latch-level radiation hardening-by-design (RHBD) techniques in a third-generation SiGe IC platform [3]. That initial SEU hardening success came, however, at the expense of large added circuit complexity and power dissipation, each with undesirable overhead. A logical question arising from that work was whether there exists other, perhaps improved, circuit-level RHBD latch designs that might simultaneously mitigate SEU sensitivity, without the overhead incurred in existing approaches.

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In the present work, a novel low-voltage high-speed SiGe latch (LVL) [4] has been modified to achieve significantly improved SEU immunity. As shown in [4], for non-SEU environments, significant power reduction can be achieved over conventional master-slave latch designs via reduced transistor stacking (as opposed to that found in standard CML architectures), while simultaneously maintaining high speed operation. Our previous SEU investigations identified that the cross-coupled storage cell was the most SEU sensitive portion of a latch [3]. In the present work, we propose a new SiGe RHBD circuit architecture using partial decoupling in the storage cell. This novel storage cell significantly improves the SEU performance of the latch, while incurring a much lower power penalty than the dual-interleaved (DI) [3], current shared hardening (CSH) [5], and gated-feedback cell (GFC) [6] approaches and requires fewer additional transistors (compared to an unhardened version) than either CSH or GFC approaches. The technique has also been applied to conventional CML, with encouraging results. The functional validity of the present SiGe SEU-hardening approach has been verified via simulation in state-of-the-art 200 GHz SiGe technology (IBM 8HP) [7], using calibrated 3-D TCAD simulated ion-strike current waveforms [8]. SEU-free operation is simulated up to data rates as high as 25 Gbps.

II. Circuit Topologies

A. Standard Low Voltage Logic

The standard low voltage logic latch is depicted in Fig. 1. The critical nodes for investigating the SEU tolerance of this circuit are Q and $\bar{Q}$, as verified via ion strikes on all circuit nodes. An ion strike to either M_1 or M_2 leads to an upset in the latch output over multiple clock cycles. This is a direct result of the strong positive feedback of the cross-coupled pair, as well as the current steering between the two storage transistors. Assuming that node Q is high and node $\bar{Q}$ is low, prior to an ion strike on M1, almost all of the tail current of the storage cell flows through M2 (since the node $\bar{Q}$ is in the "low" logic state). The ion strike changes the state of Q from a logical high to a logical low, causing the base of transistor M2 to be driven to a low state. The tail current is subsequently steered from M2 to M1 (which is in the opposite state), and thus the node $\bar{Q}$ now is forced "high," leading to an upset in the output of the latch—an SEU event.

B. Standard CML

The standard CML flip-flop is depicted in Fig. 2. Prior investigations of this topology ([2], [3]) have identified the cross-coupled storage cell as the critical node with respect to SEU. The upset mechanism in the storage cell following an

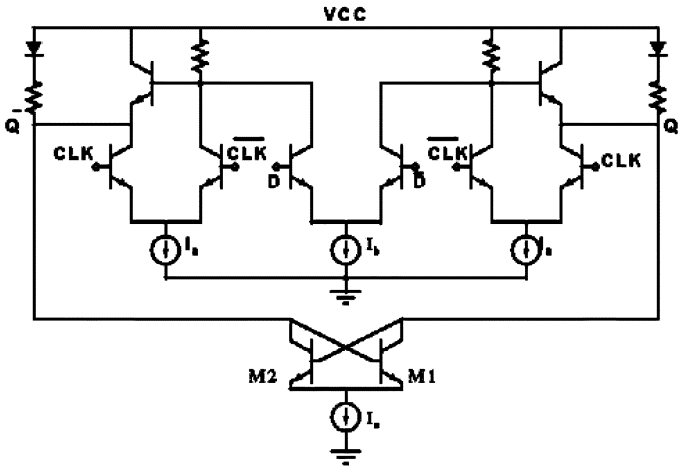

Fig. 1. Schematic diagram of Low Voltage Logic latch.

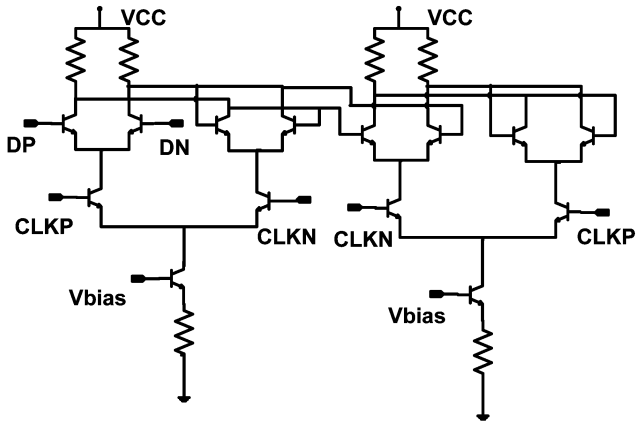

Fig. 2. Schematic diagram of a standard CML flip-flop.

ion strike is similar to the mechanism discussed in the case of the LVL topology. One important distinction is the fact that, unlike CML topology, the storage cell in the LVL topology is driven by emitter followers. The result is that the accumulated charge in the device is likely to be dissipated to the power rail much faster in case of LVL when compared to CML as a result of the very small impedance presented to it by the emitter followers. Moreover, the storage cell in the low-voltage logic is composed of transistors 1/3 the size of transistors in the pass cell, reducing the likelihood of a direct ion hit inside of the deep trench (DT) as well as the amount of charge collected in the event one does occur. This can be contrasted to the standard CML implementation, in which both the pass and storage cell transistors are of the same size.

C. SEU-Hardened Low Voltage Logic

The hardened version of the LVL latch is depicted in Fig. 3. In the unhardened version, the tail current ($\mathrm{I_s} = 0.5$ mA) of the storage cell is much smaller than that of the pass cell ($\mathrm{I_a} = 2.5$ mA and $\mathrm{I_b} = 1.5$ mA). Therefore, adding redundancy to the storage cell incurs less power penalty than duplicating the entire latch as in [3], or using CSH or GFC approaches [5], [6]. In the modified storage cell, transistors M2 to M7 are used to achieve de-coupling. In the unhardened circuit, an upset is caused when

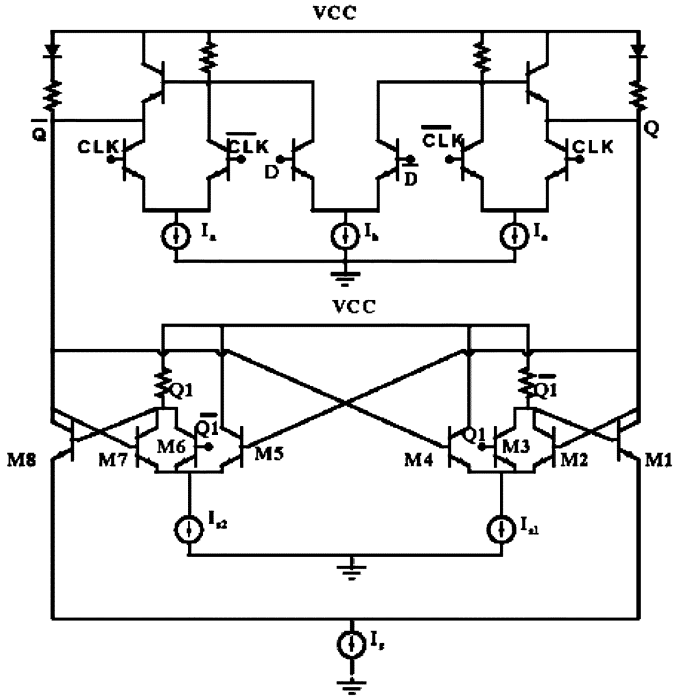

Fig. 3. Schematic diagram of SEU hardened Low Voltage Logic.

the current is shifted from the node at the low logic state to the node at the high logic state. In the modified storage cell, however, this possibility has been minimized. That is, in the hardened version, we assume that M1 is hit when Q is in the "high" state. Prior to the strike, transistors M2 and M3 are both turned on. The node Q goes low after the hit and turns transistor M2 off. Transistor M3, however, still remains in the low state and sinks all of the $\mathrm{I_{s1}}$ current. The current through the resistor connected to M2 and M3 remains the same, holding the state of $\bar{Q}1$ low. The current is thus transferred to a device in the same state rather than to an opposite state, preventing an upset at $\bar{Q}1$ and hence at $\bar{Q}$. The result is that the succeeding stage (which is also differential) can reconstruct the data using the difference between Q and $\bar{Q}$. The hardened version of this circuit preserves the reduced transistor stacking of the unhardened version, enabling it to work at low voltages without a speed penalty. The power penalty of this RHBD approach is only 14.3%, compared to 100% in DI and 300% in GFC. The transistor count and layout area are also significantly reduced when compared to current SiGe SEU mitigation techniques.

D. SEU-Hardened CML

As previously stated, the same technique can be adopted for a standard CML latch (Fig. 4). The hardened circuit shows measurable improvement in SEU as compared to the unhardened version, but reduced SEU mitigation for moderate LET ion hits compared to LVL.

One possible explanation is that the technique shields one node of the differential data from the effects of ion hit on the complimentary node. Therefore, any succeeding differential stage can easily reconstruct the data. In the low voltage logic the voltage at the affected node is quickly pulled up by the emitter followers to a level above the logic '0' and simultaneously the SEU hardening network prevents the effects of the hit from

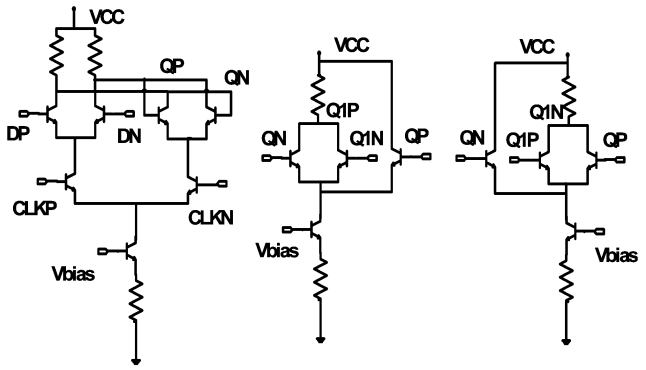

Fig. 4. Schematic diagram of CML hardened with the proposed technique.

propagating to the other node. Thus the succeeding stages are able to correctly identify the actual data.

Moreover, the excursion of the voltage at the node hit is limited as the transistor has no other transistor stack below it. However, in case of CML the voltage excursion of the node hit is well below the level of logic '0' for a period of time as a result of the lack of emitter followers to pull it up and also because of the presence of transistor stacking below it which allows a much bigger fall voltage level. Hence even though the SEU hardening network does shield the other node from effects of the hit, the succeeding stage cannot correctly identify the data at this point.

The SEU performance of the hardened CML is still better than the unhardened version. This is because as soon as the voltage level of the node hit returns to a value above logic '0' the next stage can identify the data correctly as the opposite node still has the correct data. Thus, the difference between the nodes provides the correct logic. In case of the unhardened CML the data at the node complementary to the one hit is also reversed because of the strike and it stays that way until the level at the node which was hit crosses the data threshold. The result is that it takes much longer time to correct the SEU.

III. Simulation Results

To validate the SEU hardening approach, calibrated TCAD simulations [8] were used to obtain the terminal upset currents corresponding to a heavy ion strike at a linear energy transfer (LET) values of 0.1 pC/μm, 0.2 pC/μm and 0.5 pC/μm. These time-domain upset currents were then incorporated into the Spectre simulator in Cadence in a similar fashion to that reported in [2]. The LET of 0.1 pC/μm failed to produce any upset even with the CML, hence the results are not presented here and the LET is designated as a "low LET" ion hit. The LET of 0.2 pC/μm did not cause an upset with the LVL but affected the CML hardened version. This is designated as "moderate LET" ion hit. The LET of 0.5 pC/μm caused an upset even with the hardened LVL. This is designated as a "high LET" ion hit.

The simulations were performed with a single flip-flop and with an 8-bit shift register both for the LVL and CML topologies. No significant difference was observed between the flip-flop-level and register-level upset sensitivity; therefore, we will concentrate on register-level upset results.

A. Moderate LET Single-Ion Hit (LVL and CML)

Figs. 5–7 show circuit simulation results of the hardened versus unhardened LVL register at data rates of 12.5 Gbps, 20 Gbps and 25 Gbps (corresponding to clock rates of 25 GHz, 40 GHz and 50 GHz) and at an LET of 0.2 pC/μm. The ion-strike-induced transient current was triggered in all of the circuits at 5 ns.

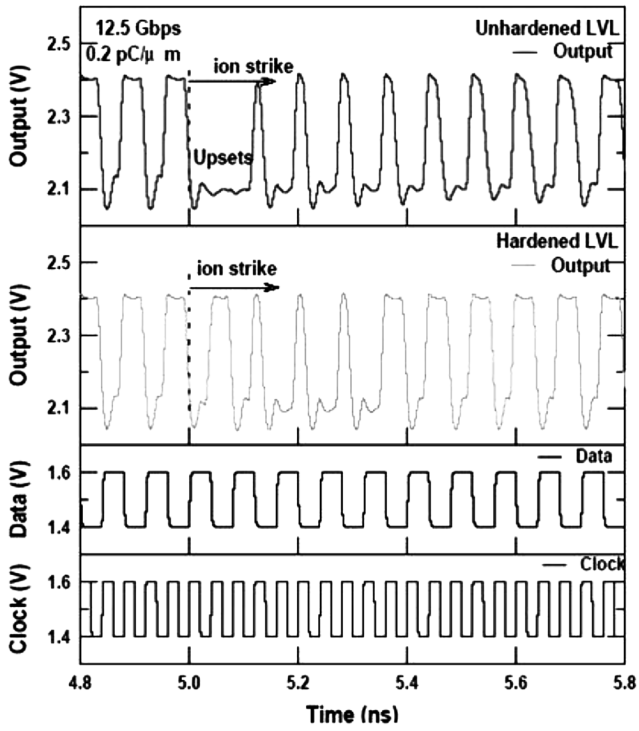

Fig. 5. Simulation result of output, data and clock waveforms of unhardened (top) and hardened (2nd from top) LVL circuits at a 12.5 Gbps data rate (LET = 0.2 pC/μm).

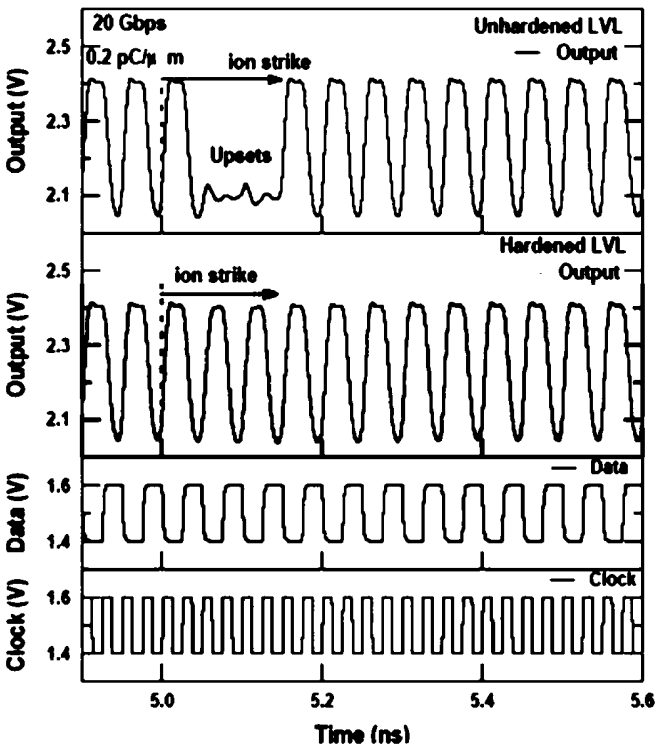

Fig. 6. Simulation result of output, data and clock waveforms of unhardened (top) and hardened (2nd from top) LVL circuits at a 20 Gbps data rate (LET = 0.2 pC/μm).

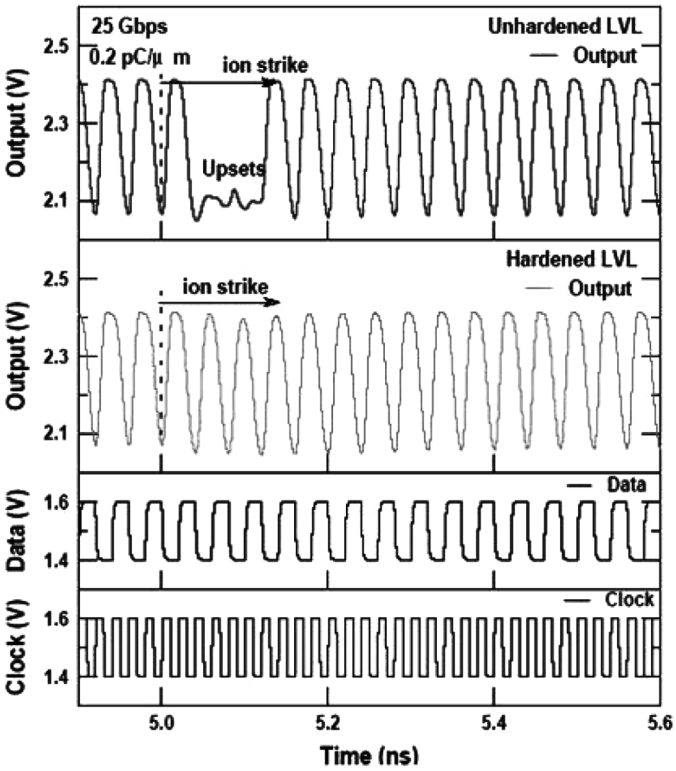

Fig. 7. Simulation result of output, data and clock waveforms of unhardened (top) and hardened (2nd from top) LVL circuits at a 25 Gbps data rate ($\mathrm{LET} = 0.2\ \mathrm{pC}/\mu\mathrm{m}$).

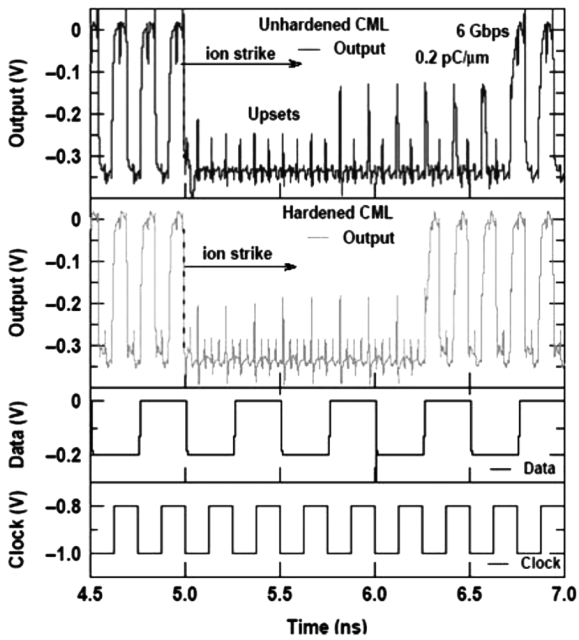

Fig. 8. Simulation result of output, data and clock waveforms of unhardened (top) and hardened (2nd from top) CML circuits at 6 Gbps data rate ($\mathrm{LET} = 0.2\ \mathrm{pC}/\mu\mathrm{m}$).

The register level simulation results of the hardened vs. unhardened CML at 6 Gbps data rate is shown in Fig. 8. In order to have a fair comparison, the power dissipation in both Low Voltage Logic and CML are kept the same. Unfortunately, with the same amount of power as LVL, the CML topology was limited to a maximum speed of 6 Gbps data rate. Although the results are not as good as for the low voltage logic, it is still measurably better.

B. High LET Single-Ion Hit (LVL)

The simulation results with moderate LET ions failed to cause any upset in the LVL hardened version. Hence the simulation was done with an LET of 0.5 pC/μm. At this LET the hardened version just starts to show upsets. Moreover, the upsets start only above a data rate of 12.5 Gbps. The simulation results show only 2 bit upset at 12.5 Gbps data rate. The dramatic improvement in SEU over the unhardened version is evident from the simulations (Fig. 9).

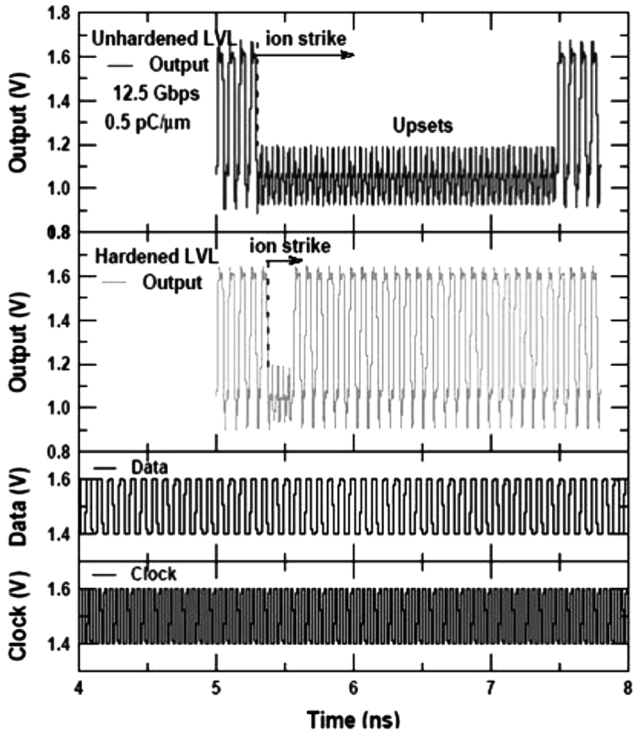

Fig. 9. Simulation result of output, data and clock waveforms of unhardened (top) and unhardened (2nd from top) LVL circuits at a 12.5 Gbps data rate for ($\mathrm{LET} = 0.5\ \mathrm{pC}/\mu\mathrm{m}$).

C. Moderate LET-Multiple-Ion Hits (LVL)

To gain further insight into the working and the limitations of the approach, simultaneous hits to multiple transistors of the storage cell of both the hardened and unhardened LVL have been simulated at an LET of 0.2 pC/μm.

Fig. 10(a) shows the simulation results of simultaneous hits on both the transistors of the cross-coupled cell of the unhardened LVL. As the transient currents are equal in both of the branches, the effect of the signal is a common-mode to the succeeding differential stage, which rejects it. Hence the output of the register remains unperturbed.

Fig. 10(b)–(d) are the simulation results of two ion hits on the hardened LVL for various combination of nodes of the storage cell. Fig. 10(b) shows the results of hits to the nodes Q and $\bar{Q}$ simultaneously. Again the same effect, as observed in the case of unhardened LVL, occurs. Thus we can conclude that if there are simultaneous hits to nodes which are complementary

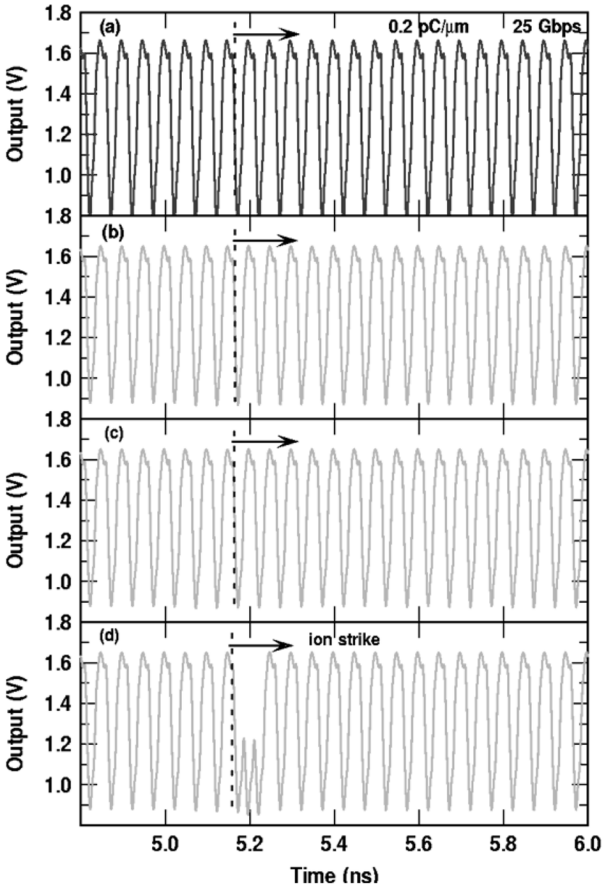

Fig. 10. Simulation result of two ion hits (each LET $= 0.2pC/\mu$m) (a) Hits on storage cell transistors of unhardened LVL (b) Hits on the nodes Q and $\bar{Q}$ of hardened LVL (c) Hits on the nodes Q and $\bar{Q}1$ of hardened LVL (d) Hits on the nodes Q and $Q1$ of hardened LVL.

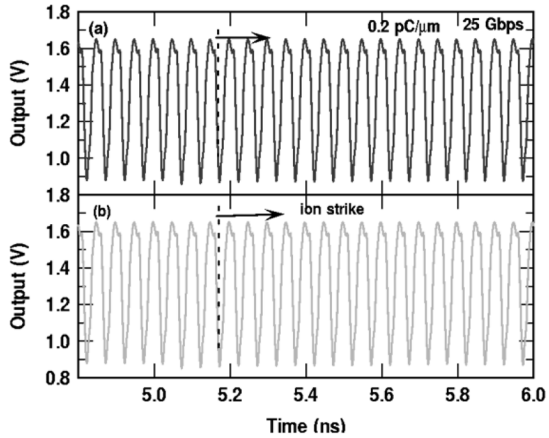

Fig. 11. Simulation result of the hardened LVL register for ion hits on (a) Three nodes of the storage cell (b) Four nodes of the storage cell.

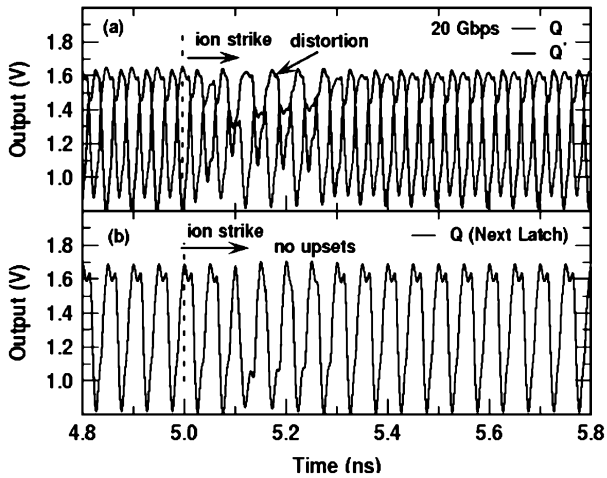

Fig. 12. The output waveform of the latch hit (LVL) and the latch succeeding it. The waveforms show how a hit distorts the node hit, but the complementary node is not affected thus allowing the next stage to completely reconstruct the data.

to each other in logic, the effect will be rejected by the next stage. Fig. 10(c), which shows the simulation results of hits on the nodes Q and $\bar{Q}1$ offer further support of this theory.

Fig. 10(d) is the simulation result of hits on Q and $Q1$. The hardening network was designed to prevent upset from occurring in the case of a single ion hit, which generally is the predominant cause of upsets. The two hits to the above two nodes disrupts the corrective action of the network, which needs at least one correct result from either Q or $Q1$. Hence now both the other two nodes $\bar{Q}$ and $\bar{Q}1$ suffer bit-flips leading to an upset.

Figs. 11(a)–(b) show the simulation result of three and four ion hits to the hardened LVL respectively. No upset is observed in either case. A plausible explanation may be that since from among the three nodes hit, at least two are always complementary nodes, and the effect of an ion hit to these two are rejected. Thus the three ion hit case becomes almost equivalent to the single ion hit case, which the circuit can effectively mitigate. In case of the four ion hit case where all the nodes of the storage cell of the hardened LVL i.e., $Q, Q1, \bar{Q}$ and $\bar{Q}1$ are hit, the effect of the hit are rejected due to the common mode rejection, as discussed above.

IV. Analysis of Results

The simulation results clearly show remarkable improvement in SEU performance of the hardened version compared to the unhardened version in case of LVL. Fig. 12 shows the differential output (Q & Q* of a latch (LVL) hit and then the output of the latch succeeding it (Q only) for a moderate ion hit. It is evident how Q is distorted when it is hit by a ion but Q* stays at the correct level. The next stage which needs only 20 mV of difference to identify the data can then successfully regenerate it. Hence the Q output of the next stage shows no effect of SEU.

Fig. 13 shows a plot of the difference between hardened and unhardened circuit in terms of bits lost to SEU over different data rates.

Table I compares the different SEU techniques with respect to their power penalty and transistor count, compared to their corresponding unhardened versions. The proposed technique has the lowest transistor count penalty with the smallest power penalty.

V. Summary

The results suggest that the new SEU-hardened low voltage latch topology is an ideal candidate for use in space environments. Not only does it have the capability to operate over a very large bandwidth and support very high data rates, but it also has

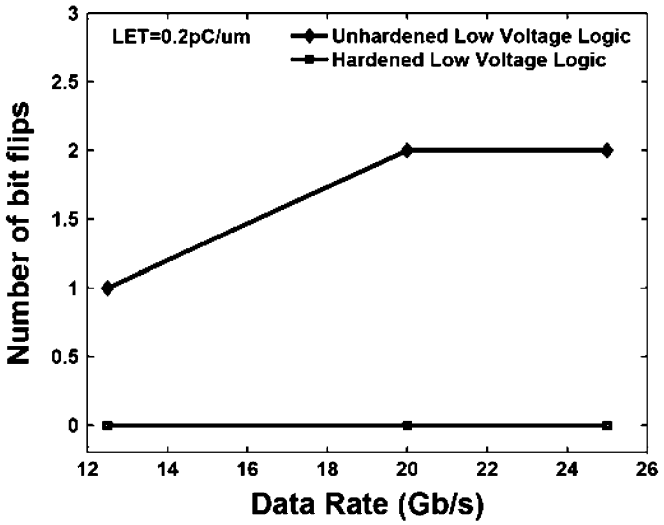

Fig. 13. A comparison of number of upsets due to ion strike (0.2 pC/μm) on hardened and unhardened Low Voltage Logic. The data rates are 12.5, 20 and 25 Gbps.

the advantage of low-voltage/low-power operation. This SEU hardening technique can also be easily incorporated on existing CML with minimal effort on the part of the designer while providing it with moderate SEU immunity.

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TABLE I
COMPARISON OF DIFFERENT SEU HARDENING TECHNIQUE WITH RESPECT TO THEIR INCURRED PENALTY OVER THEIR UNHARDENED VERSIONS

Metric	Dual-Interleaved [2]	Current Shared [4] [7]	Gated Feedback [2]	**This work (For LVL)**
Power Penalty	100%	None	300%	14%
Area Penalty	60%	N/A	150%	50%
Penalty in Transistor Count	100%	400%	157%	80%
Supply Voltage (V)	3.3-4.0	3.3-4.0	3.3-4.0	2.0-2.5

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